IC Design Planning Method and System

Abstract

An IC design planning method and a system thereof for providing minimized path delay and routing congestion of an IC design are disclosed. The IC design planning system includes a sub-block decoder that is capable of decoding sub-block level information and explicitly consider critical paths of sub-blocks in the sub-block placement and pin positioning processes within a block. The sub-block placement process involves calculating sub-block placement parameters such as weight, center of mass and orientation of a critical pin set of each sub-block for deciding on the order of sub-block selection and placement. The pin positioning process involves finding a preferred pin position for positioning each pin on the boundaries of the sub-blocks.